IDEC Chip Design Contest

An 82fs$_{RMS}$-Jitter 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency Multiplier-Based Phase Detector

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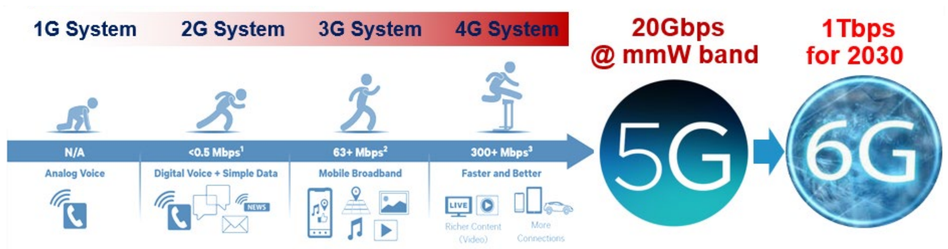
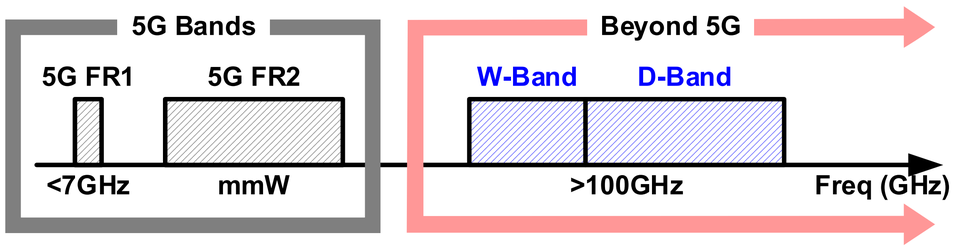
Motivation



- To accommodate exponentially increasing data-traffic, the data rates of mobile communication systems are rapidly increasing

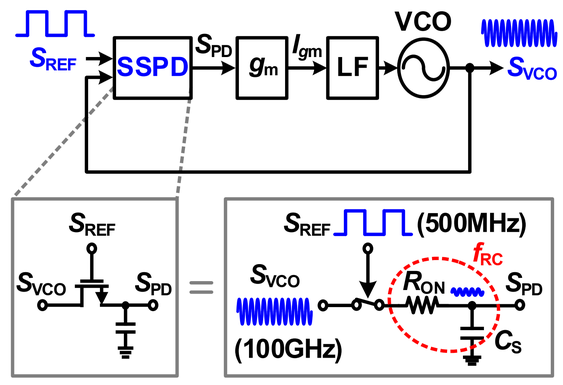


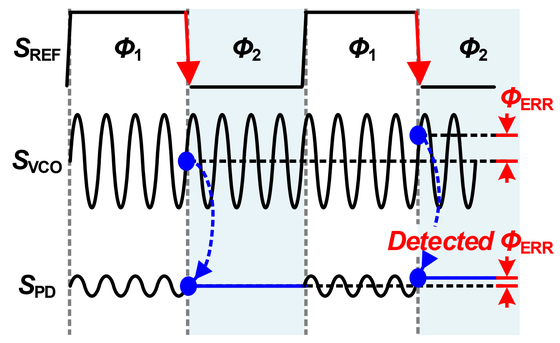
- For higher data rates for beyond 5G, even higher-frequency bands need to be considered to use wider bandwidth

→ Need to explore W-band and D-band

Problems of Prior Architectures

❖ Conventional W-Band PLL using Sub-Sampling Phase Detector (SSPD)





- In W-band, amplitude of S_{PD} is reduced by parasitic RC pole (f_{RC}) of PD switch

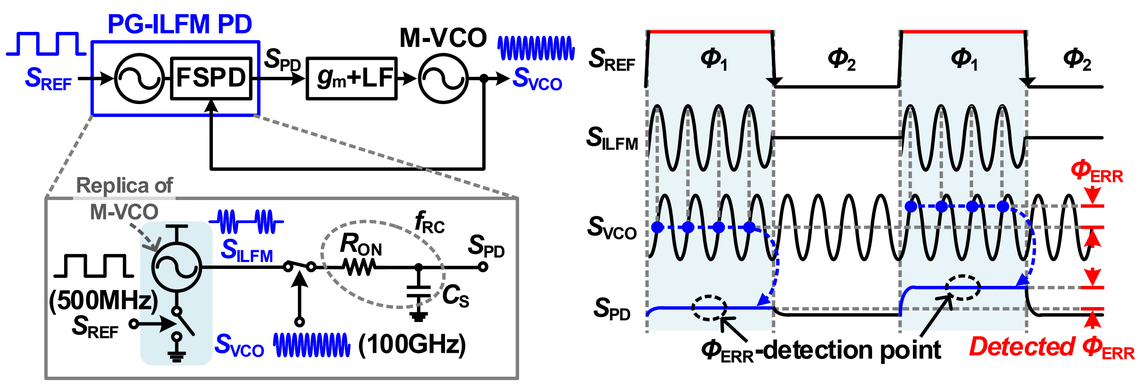
→ Φ_{ERR}-detection gain of PD decreases

→ In-band phase noises from SSPD, g_m, LF increases

→ Since W-band VCO also has poor phase noise, PLL cannot achieve low jitter under 100fs ☹

Concept of Proposed Idea

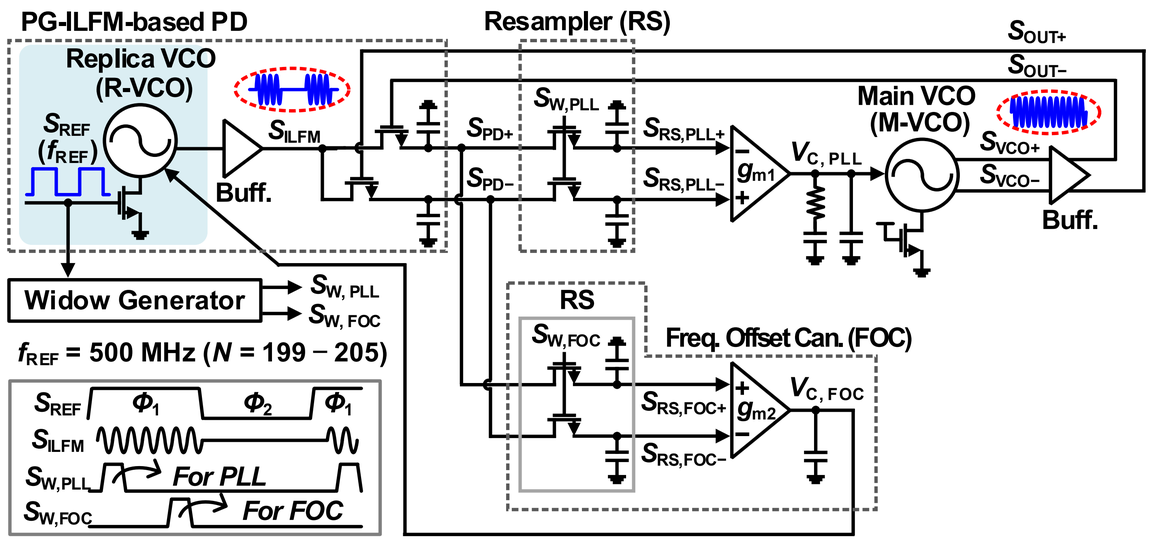
❖ Proposed W-Band PLL using Power-Gating ILFM-based PD



- Fundamental sampling PD (FSPD): sampling S_{VCO} with S_{ILFM} having same W-band frequency
- Using FSPD, Φ_{ERR} information can be detected without any loss due to the RC pole of PD switch

➔ Power-gating ILFM-based PD can take advantages of FSPD with low reference clock such as 500 MHz ☺

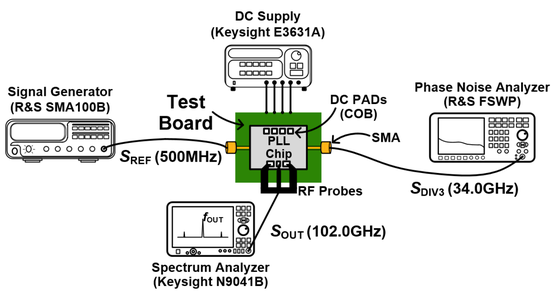
Architecture of Proposed W-Band PLL



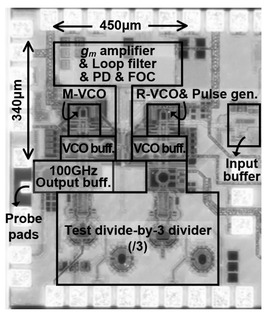
- Main PLL consists of PG-ILFM-based PD, RS, g_m amplifier, LF, and Main VCO to remove Φ_{ERR} of PLL output
- Freq. Offset Canceller (FOC) consists of RS and g_m amplifier, and LF to cancel freq. offset btw. Main and replica VCOs

Measurement Results

❖ Measurement setting



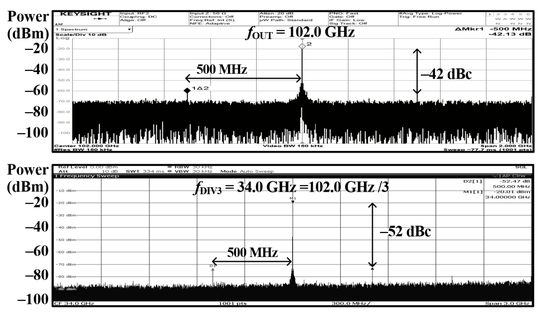
❖ Die photograph



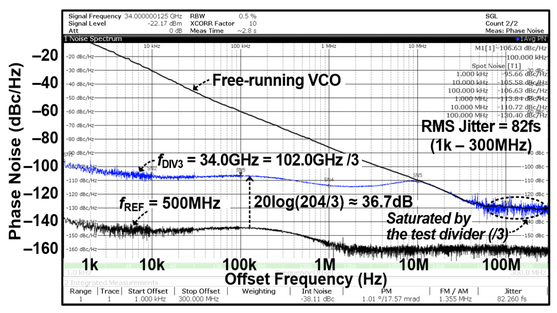
❖ 65nm CMOS
❖ Active area: 0.16mm²
❖ Power: 22.5mW

Power Consumption (mW)	
M-VCO	8.0
R-VCO	4.5
Gm amplifier & PD & FOC	2.0
VCOs' buffers	7.0
Start-up Pulse gen.	1.0
Total	22.5

❖ Measured spectrum



❖ Measured phase noise



Performance Comparison

	This work	ISSCC'09 K. Tsai	TMTT'14 S. Kang	ISSCC'18 Z. Huang	RFIC'14 Y. Chao	VLSI'19 X. Liu
Process	65nm CMOS	65nm CMOS	130nm SiGe	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	PG-ILFM-based PD Direct W-band PLL	Direct W-band PLL	Direct W-band PLL	Direct W-band DPLL	50GHz PLL + Push-push(x2)	23GHz PLL + ILFM (x4)
Type	Integer-*N*	Integer-*N*	Integer-*N*	Integer-*N*	Integer-*N*	Integer-*N*
Supply (V)	1.2/ 0.8	1.2	3.3/ 2.5/ 1.2	1.2/ 0.8	1.2/ 0.6	N/A
Output Freq, f_{OUT} (GHz)	99.5 – 102.5	95.1 – 96.5	92.7 – 100.2	82.0 – 107.6	96.8 – 108.5	80.0 – 104.0
Reference Freq, f_{REF} (MHz)	500	375	1500	125	195	100
Multiplication Factor (*N*)	199 – 205	256	64	656 – 864	512	800 – 1040
Reference Spur (dBc)	−42	−52	< −60	< −34	−40	−40
1MHz PN (dBc/Hz) @ f_{OUT} (GHz)	**−104.3 @102**	**−75.7 @95.5**	**−102.0 @95.0**	**−79.0 @107.6**	**−88.0 @99.4**	**−93.0 @100.8**
Jitter$_{RMS}$, σ_t (fs)	**82 (1k – 300MHz)**	**2220 (1k – 10MHz)**	**71 (1M – 1GHz)**	**278 (1k – 10MHz)**	**170* (10k – 10MHz)**	**137 (10k – 10MHz)**
Power, P_{DC} (mW)	22.5	43.7	469.3	35.5	14.1	23.6**
Active Area (mm²)	**0.16**	**0.70**	**0.93**	**0.36**	**0.39**	**0.41****
FOM$_{JIT}$*** (dB)	**−248.2**	**−216.7**	**−236.2**	**−235.6**	**−243.8**	**−243.5**

*Calculated from the PN graph in Fig. 8 of [RFIC'14, Y. Chao] **Power and area only for the W-band ***FOM$_{JIT}$ = 10log($\sigma_t^2 \cdot P_{DC}$)

☺ The proposed W-band PLL achieved the FOMJIT of −248.2dB, which is the best among the state-of-the-art W-band frequency synthesizers

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